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Advanced Flip Chip Bonding Techniques Using Transferred Microsolder Bumps

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bstract

For future high-speed and high-density OE-MCM (opto-ectronic multi-chip module) packaging, a technique will be eded that can bond several high-speed photonic devices d LSIs onto an OE substrate using various heat-treatment ocess and can allow control of the device's position for tical alignment and high-density packaging. In the present ork, we produce two advanced transferred microsolder bump nding techniques for high-speed and high-density OE-MCM ckaging. One uses 80% Au-Sn transferred microsolder mp bonding. This material allows module packaging ng processes at various temperature because it has a higher lting temperature than 100% In and 60% Sn-Pb solder. e other technique uses multi-transferred microsolder bumps de using a repeated transfer process. It can offer accurate ee-dimensional flip-chip bonding because it provides cise vertical and horizontal alignments within the errors of).5 μm. These techniques will thus be very useful in eloping the high-speed and high-density OE-MCM for lti-functional boardlevel interconnection in future optical mmunication systems.

oduction

Future broadband Integrated Service Digital Networks (B-N) will require asynchronous transfer mode (ATM) ching systems having total throughputs of more than 1 /s. Developing such high-speed ATM system will ire high-density multi-chip modules with throughputs of several hundred Gbit/s at the boardlevel interconnection. chieve such high-speed interconnection modules, we have developed OE-MCM packaging using organic optical eguides formed on copper-polyimide (Cu-PI) multi-layer trates. Figure 1 is a schematic representation of high- d and high-density OE-MCM packaging that we have ously reported [1].

accomplishing such OE-MCM packaging as shown in l, high-speed, highly integrated LSI chips will continue key devices for high-throughput modules, even after al interconnection comes into use. High-density ging to reduce electrical interconnection delay will still quired, because the number of LSI I/Os is increasing. the OE-MCM technologies require a defect-free solder bump bonding technique for LSI and photonic es to transfer Gbit/s-order electrical signals [2], a que for multi-chip bonding onto the same substrate by several different solder materials in treatments at s temperatures, and controllability of device position for l alignment between the optical fiber/ the waveguide ser-diode/ photo-diode.

the past, we formed the microsolder bumps by direct phase deposition of the solder at the electrodes in the n area of the photonic devices. One concern with this ch was the damage that could occur due to stress during the vapor-phase deposition. To prevent such damage and to realize high-density interconnections, we have developed a defect-free flip-chip-bonding technique that uses 100% In and 60% Sn-Pb transferred microsolder bumps[3]. This technique can simplify the fabrication process because the bump-formation process is separate from the device processes. Moreover, even if the transfer of the bumps cannot be completed in one pass, this technique can still achieve perfect bump bonding by re-transferring. It can also provide efficient flip-chip bonding because it can be applied selectively only to the defect-free devices.

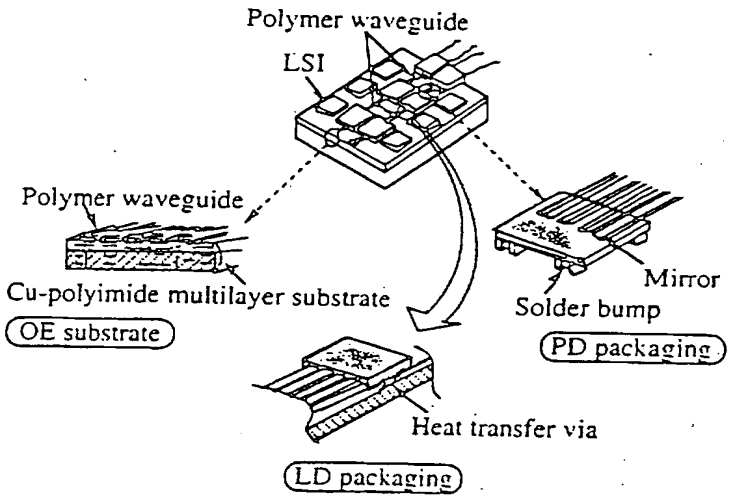

Fig. 1. Schematic representation of LD and PD packaging in OE-MCM[1].

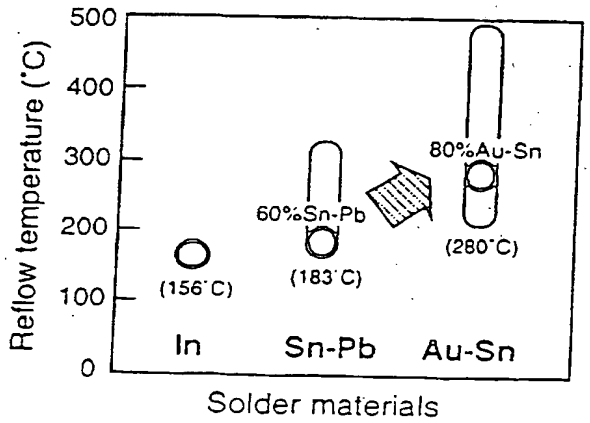

Fig. 2. Reflow temperature dependence of solder materials.

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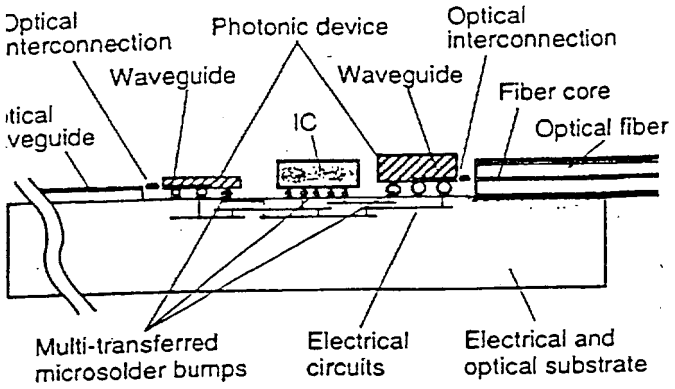

g. 3. Optical packaging application using multi-transferred microsolder bumps.

Here, we report on our investigation of two advanced nsferred microsolder bump bonding techniques for high- ed and high-density OE-MCM packaging. One uses 80% -Sn transferred microsolder bump bonding. Figure 2 ows the reflow temperature dependence of the solder terials. This technique can provide module packaging t involves treatments at various temperatures and affords lti-chip bonding on the same substrate, because 80% Au- has a higher melting temperature than the 100% In and % Sn-Pb solder.

The other technique uses multi-transferred microsolder mps, i.e., bumps made using repeated transfer. In its tial state the microsolder bump has the capability of precise f-alignment in the substrate plane with the error of ± 0.5 [2]. The multi-transferred microsolder bump bonding hnique allows control of the diameter of solder bumps, to vide not only in-plane alignment but also three- nensionally accurate flip-chip bonding.

Figure 3 shows one example of optical packaging lications that can be produced using multi-transferred crosolder bump bonding technique. Currently, in the gnment of the optical fibers and photonic devices, their ght is controlled by changing the height of the device tform and the shape of the V groove. The tolerance of the gle-mode optical fiber alignment is about ±2 or 3 μm at one tional axis. By using the technique, it is possible to trol device heights by changing the bump diameter within tolerance of the fiber alignment. These two techniques l thus be very useful in the development of the high speed l high density OE-MCMs for future high-speed optical nmunication systems.

atures of Transferred Bump Bonding Technique

The basic procedure for fabricating transferred microsolder nps (formation of the deposited solder, transfer of the crosolder bumps, and bump bonding) is shown in Fig. 4. st the solder-bump pattern is formed on the carrier strate, using a thick photoresist (b). Then the solder is osited by vapor-phase deposition (c). Next the deposited der bumps are formed on the carrier substrate by lifting off photoresist (d). A chip with a base-metal pattern is then ned face-to-face with the deposited solder bumps (e), and solder bumps are transferred by applying a slight pressure eflow the solder (f).

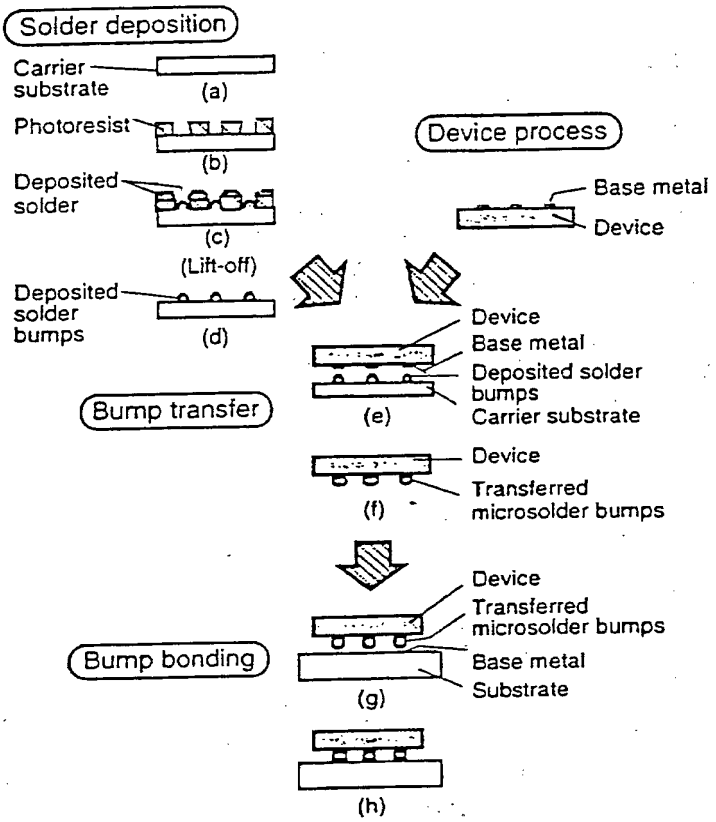

Fig. 4. Basic process of transferred microsolder bumps.

Finally, the chip with the transferred microsolder bumps is aligned face-to-face with a wettable base metal on a substrate (g), and is flip-chip-bonded onto the substrate (h).

Thus the transferred microsolder bump bonding technique has several benefits, as follows. First, damage to devices caused by stress during solder deposition is prevented because the bump-formation process is separate from the device formation. Second, simultaneous formation of many different carrier substrates with various chip sizes and bump pitches on a single Si wafer makes many applications possible. Last, the chips with transferred microsolder bumps are applied only to defect-free device, because carrier substrates with the deposited solder are individually aligned face-to-face with the base metal on the devices.

Transferred Bump Bonding Using 80% Au-Sn Solder

A. Test sample structure

The test sample structure and bump arrangements are shown in Table 1 and Fig. 5. The samples consisted of a 2-mm-square Si chip and a 2-mm-square Si carrier substrate. The wettable base metal was formed lithographically on the Si chip: Ti/Pt/Au was used as the base metal, whose total thickness was about 0.3 μm. A wafer of Si, which is a non-wettable material, was used as the carrier substrate. There were 131 microsolder bumps, each with a diameter of about 40 μm arrayed in a 120 x 200 μm area on the 2-mm-square substrate. We used 80% Au-Sn solder as the bump material.

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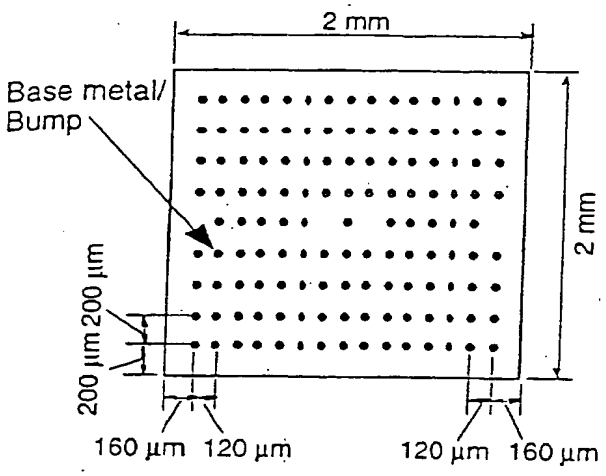

Fig. 5. Arrangement of test sample

Table 1. Composition of chip and substrate.

Chip	Size	2 mm square
	Material	Si
	Base metal	Ti/Pt/Au (36 µm diameter)
Carrier substrate	Size	2 mm square
	Material	Si
Microsolder bump	Diameter	about 40 µm
	Pitch	120 x 200 µm
	Number	131
	Material	80% Au-Sn

abrication process

he detailed process for fabricating the 80% Au-Sn ferred microsolder bumps is shown in Fig. 6. First, a with a base-metal pattern is aligned face-to-face with the r bumps deposited on the carrier substrate (a), and the ttachment is done by applying a slight pressure (b). the carrier substrate and chip are heated on the bonding to a temperature below the melting point of the 80% n solder while a slight pressure is applied (c). Then, the ited solder bumps are reflowed at a temperature above ielting point of the 80% Au-Sn solder and transferred to ase metal of the chip (d).

Results and discussion

gure 7(a) shows a magnified view of the 80% Au-Sn erred microsolder bumps on the 2-mm-square Si chip fter transfer. Figure 7(b) shows a SEM (scanning on microscope) photograph of these bumps after reflow ng. All bumps were successfully transferred onto the ip, but they deformed a little just after the transfer. v forming allowed the bumps to form into spheres. As d-result, uniform microsolder bumps with a diameter of 40 µm were successfully transferred onto the Si chip.

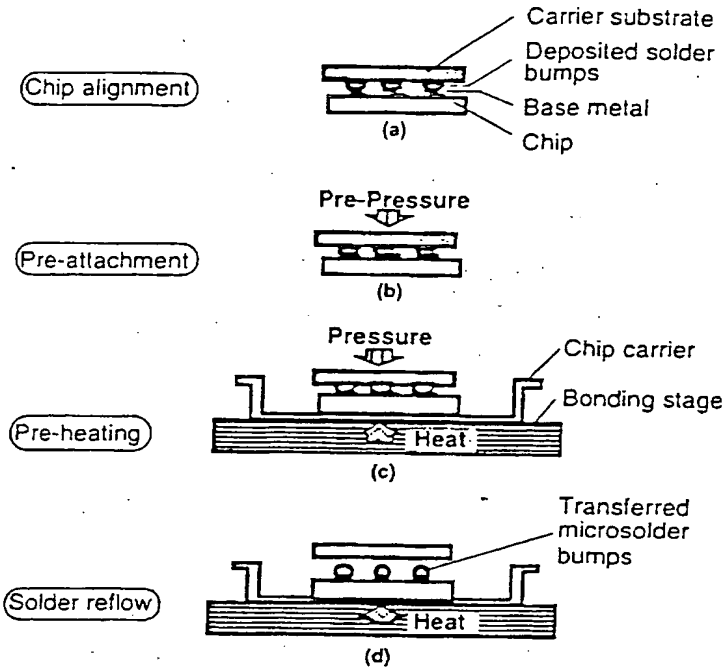

Fig. 6. Procedure for Au-Sn transferring microsolder bumps.

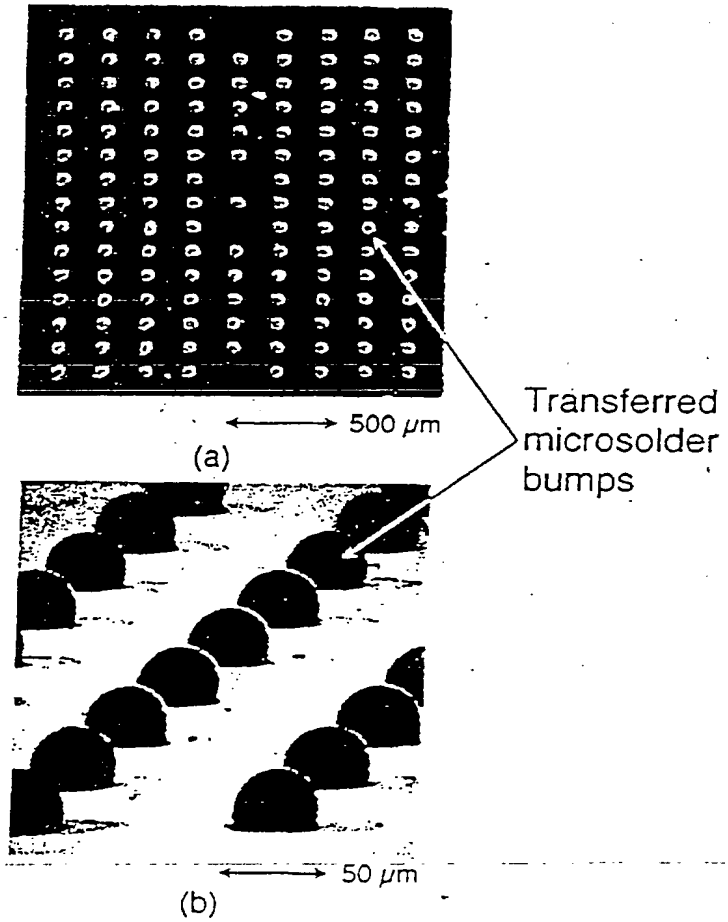

Fig. 7. Transferred microsolder bumps of Au-Sn solder: (a) after transfer; (b) after reflow forming.

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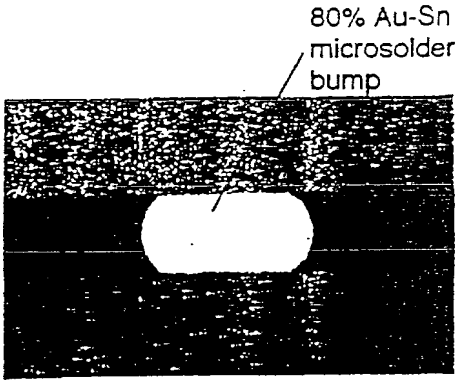
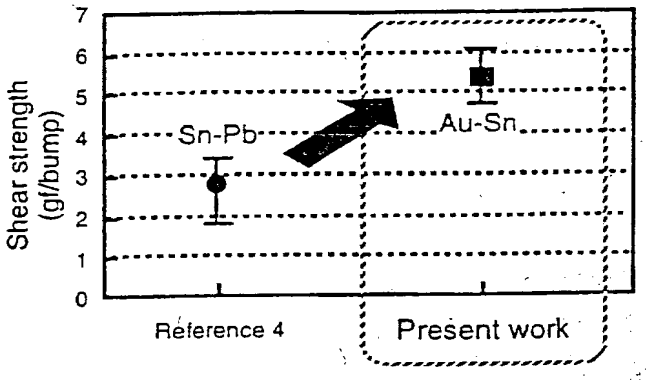


8. Cross sectional photograph of bonding test sample using 80% Au-Sn micro solder bumps.



9. Shear strength of Au-Sn transferred microsolder bumps.

The cross sectional photograph is shown in Fig. 8 after ıding the Si chip onto the Si substrate by 80% Au-Sn ısferred microsolder bumps. The shape of the bonding nps is spherical and self-alignment bonding was achieved. Figure 9 shows the shear strength after flip-chip ıding. The average shear strength of 80% Au-Sn solder s about 5.5 gf/bump, which is twice the value for Sn-Pb nps[3]. These results show that mechanically reliable and fect Au-Sn microsolder bump bonding can be achieved.

ılti-transferred Bump Bonding Using 60% Sn-Pb der

Test sample structure

The test sample structure and bump arrangements are ilar to those shown in Table I and Fig. 5. In this study, used a 60% Sn-Pb solder.

Fabrication process

Figure 10 shows the fabrication process. This technique roughly similar to the transferred microsolder bump ding technique described above, as it repeats the transfer ess to the same device using several carrier substrates h the deposited solder arranged in the same pattern. This nique can quickly make transferred microsolder bumps on device that have the same pitch but a different diameter. It also achieve more accurate vertical alignment by repeating the transfer with the deposited solder. In cases where it is not possible to fabricate solder bumps using a one-time vapor-phase deposition and/or solder transfer process, this technique can be used to produce relatively large solder bumps at a narrow pitch.

C. Results and discussion

Figure 11 is a SEM photograph of multi-transferred microsolder bumps of the same solder volume, fabricated on a 2-mm-square Si chip. Fig. 11 (a), 11(b), and 11(c) show the microsolder bumps after one, two and three time transfers, respectively. The diameter of the base metal was 36μm and the total number of bumps was 131. The diameter of the transferred bumps increased from about 40 to 60 μm with increasing transfer time, while keeping the pitches of individual bumps unchanged with increasing transfer time. This confirmed that the diameter of desired bumps can be controlled by increasing the transfer time. The test chip was bonded onto the substrate using three-times-transferred microsolders, as shown in Fig. 12.

Figure 13(a) shows the measured and calculated results for the bump height after flip-chip bonding. By transferring one, two, or three times, it was possible to control the bump heights to be between about 25 to 45 μm at most 1 μm less than the calculated one. Figure 13(b) shows the bump heights dependence of changing volume of the solder at two times transfer. By using less than 5×10^3 μm^3 solder, it was also possible to control the bump heights to be one micron step at most 0.5 μm less than the calculated one. The results showed that this technique can achieve accurate vertical alignment for microsolder bumps.

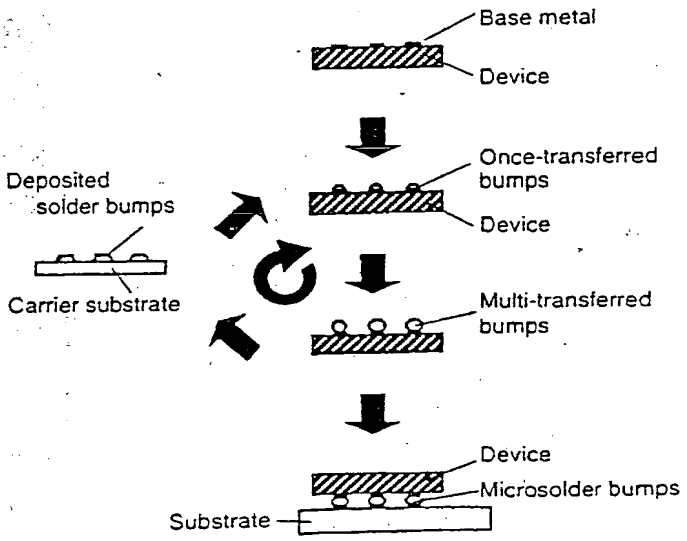


Fig. 10. Fabrication process of multi-transferred microsolder bumps.

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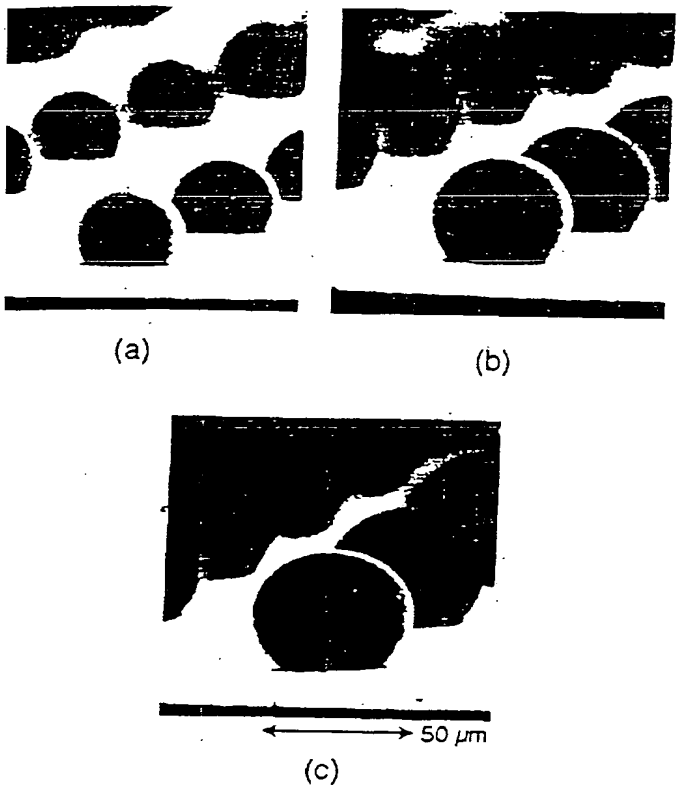
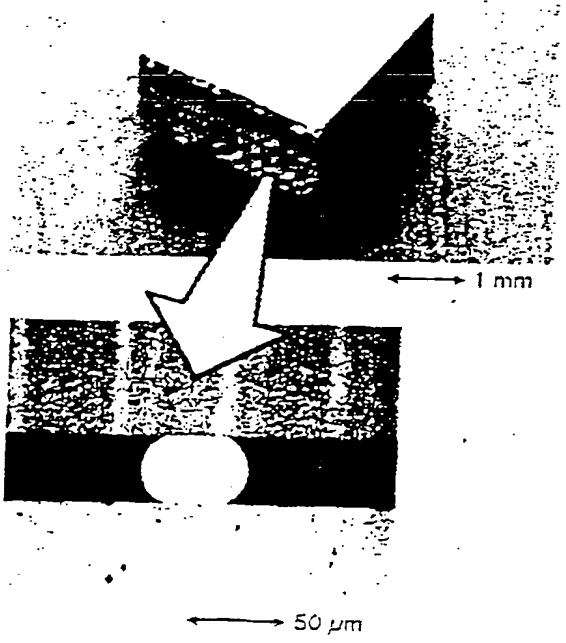


11. Multi-transferred microsolder bumps fabricated of Sn-Pb solder: (a) Once-transferred; (b) twice-transferred; (c) three-times-transferred.



Flip-chip bonded test sample using 60% Sn-Pb three-times-transferred microsolder bumps.

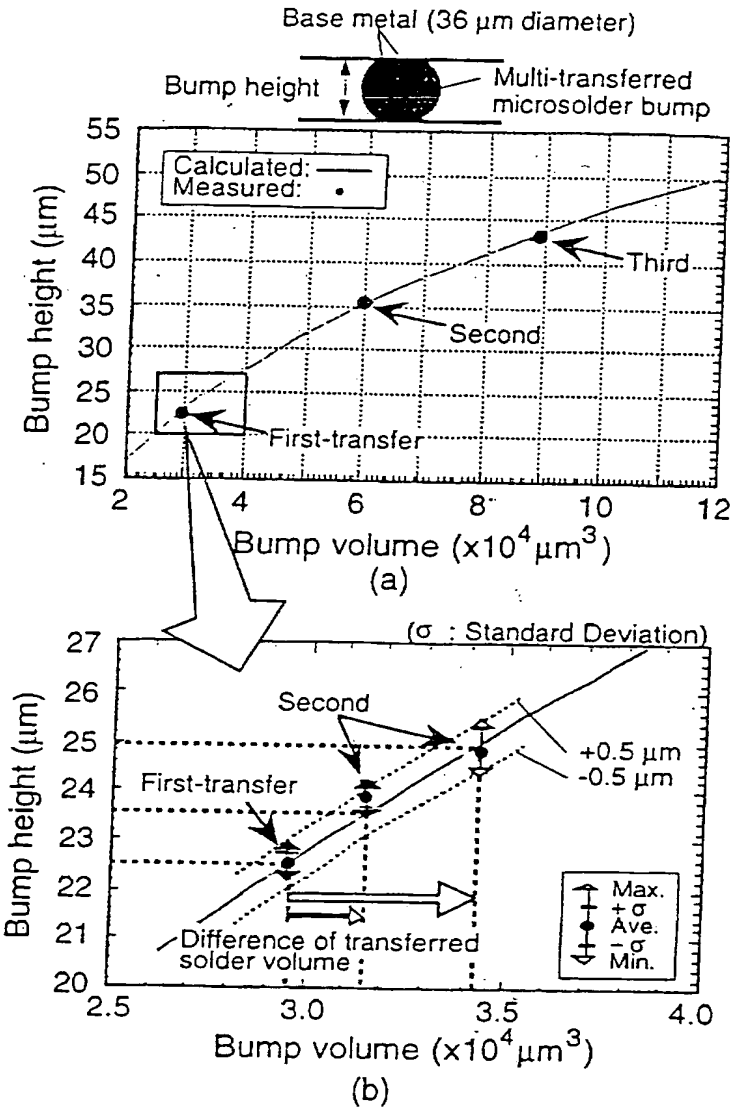


Fig. 13. Bump height after flip-chip bonding.

Conclusions

Toward developing the high-speed and high-density OE-MCM packaging, two advanced transferred microsolder bump bonding techniques were proposed.

One uses bonding transferred microsolder bumps of 80% Au-Sn, which can allow module packaging that involves heat treatments of various temperatures because it has a higher melting temperature than 100% In and 60% Sn-Pb solder. We successfully transferred 131 uniform 80% Au-Sn microsolder bumps having a diameter of 40 μm; they were made spherical by reflowing and bonded to the base metal on the Si substrate. The average shear strength of the 80% Au-Sn solder was about 5.5 gf/bump, proving that mechanically reliable and perfect Au-Sn microsolder bump bonding can be achieved.

The other technique uses multi-transferred microsolder bumps made using a repeated transfer process. By transferring one, two, or three times, it was possible to control the bump heights to be between about 25 to 45 μm at most 1 μm less than the calculated one. By using less than 5×10^3 μm^3 solder, it was also possible to control the bump heights to be one micron step at most 0.5 μm less than the calculated one.

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These techniques will be very useful in developing the high-speed and high-density OE-MCM packaging required for electrical and photonic devices with stable, high-speed, and multi-functional boardlevel interconnection needed for future high-speed optical communication systems.

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brid integrated 4×4 optical matrix switch ng self-aligned semiconductor optical plifier gate arrays and silica planar twave circuit p. 996-997 = (2)

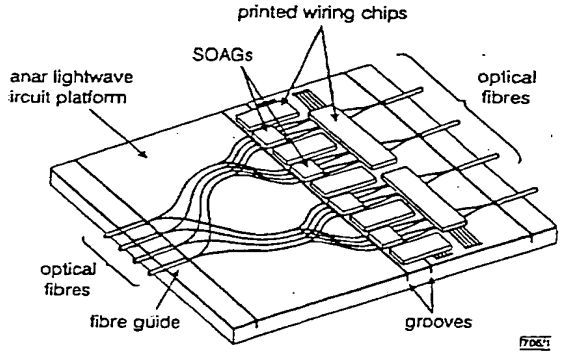
asaki, H. Hatakeyama, T. Tamanuki, S. Kitamura, Yamaguchi, N. Kitamura, T. Shimoda, Kitamura, T. Kato and M. Itoh

14-05-1998

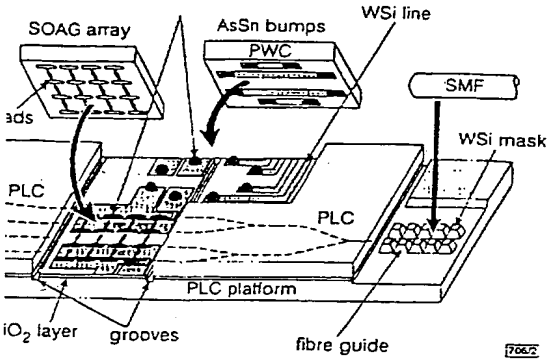
A 4×4 gate matrix switch has been developed by employing a newly developed self-aligned multiple chip assembly technique in the hybrid integration of spot-size converter integrated semiconductor optical-amplifier gate arrays and optical fibres on a silica based planar lightwave circuit platform.

duction: Large capacity switching systems based on photonic nologies hold great promise for the achievement of high ghput telecommunication networks which are able to cope large increases in traffic [1]. Such systems would require a number of photonic matrix switches for multi-channel cross-ection. Of those photonic matrix switch structures currently able, semiconductor optical amplifier gate (SOAG) based hes appear to be the most promising because of their high tion ratio, high optical gain, and fast switching time (sub-second). In terms of mass-production and miniaturisation, most suitable way of producing a practical gate type matrix n module would seem to be hybrid integration, in which mul-SOAG arrays are assembled onto a platform in combination a planar lightwave circuit (PLC), as opposed to conventional ns which require a large number of fibre components and sin-annel optical amplifier modules.

this Letter, we describe a newly developed optical hybrid ation technology assembling multiple SOAG arrays and l fibre arrays on a silica based PLC platform in a self-d manner. We have applied this technique to the fabrication ×4 optical matrix switch module in which all 16 paths suc-lly perform gate operations.



Structure of hybrid integrated 4×4 optical gate matrix switch



onfiguration of hybrid integration

structure: Fig. 1 shows the 4×4 optical matrix module. l optical splitters and four 4:1 combiners are formed on a tform, on which four-channnel SOAG array chips are also l. A singlemode optical fibre (SMF) array is assembled in des at each end of the platform. Newly developed technol-ogies for the production of this hybrid integrated module are discussed in the following two Sections.

PLC platform: Fig. 2 shows the configuration of the hybrid integration. The PLC platform requires transmission lines to drive the SOAG arrays, precise solder wettable pads for bump bonding and precise fibre guides. The PLC is partly etched to expose those areas on which the SOAGs and optical fibres are to be assembled. For protection against etching of the SiO_2 layer, which is both for insulation of the transmission lines and for use in masking during the anisotropic etching conducted to fabricate the block fibre guides [2], a WSi layer is first deposited on the SiO_2 layer. Over this, another SiO_2 layer is deposited for the PLC. If a conventional process were used for this deposition, its high temperature (> 1000°C) could damage the WSi layer; however, to avoid such damage, we employed low temperature (400°C) atmospheric pressure chemical vapour deposition (AP-CVD) using tetraethoxysilane (TEOS) as precursor [2]. The WSi layer is also used for transmission lines.

Simultaneous self-aligned assembly of multiple optical/electrical devices: We employed the self-aligned assembly technique [3, 4] which makes use of solder bumps. For high reliability and flux-free bonding, we used Au-80 wt%/Sn-20 wt% eutectic alloy solder. The solder bumps were formed by a mechanical punching method [4], providing high uniformity and low cost. The Au/Sn solder pieces were first formed by punching an Au/Sn ribbon using a micro punch and a die, and then directly pressed against the solder-wettable pads. To achieve high vertical precision, we used stripe-type solder bumps, rather than the spherical bumps usually employed in flip-chip bonding [5]. These stripe-type bumps do not suffer the height deviation due to solder volume deviation that is suffered by conventional spherical bumps. A positioning accuracy of $< \pm 1\,\mu m$ was possible in both the lateral and vertical directions.

Coupling loss between SOAGs and waveguides is ordinarily ~8-9dB. To reduce such loss, we used spot-size converter (SSC) integrated SOAG arrays [6]. Radiation divergence was 13–14° (FWHM) in both the azimuth and elevation planes, as opposed to ~40° in non-SSC devices. In this way, we kept coupling loss down to 4–5dB.

The silica waveguide facets facing the SOAGs were sawed off perpendicularly to obtain flat surfaces. However, it is difficult to create the transmission lines across the groove resulting from this sawing that are needed to connect to the SOAGs. To avoid this difficulty, we employed printed wiring chips (PWCs) to create electrical connections over the grooves as shown in Fig. 2. The PWCs and SOAGs were simultaneously mounted with solder bump reflow. This PWC technique is also applicable to the assembly of driver IC chips.

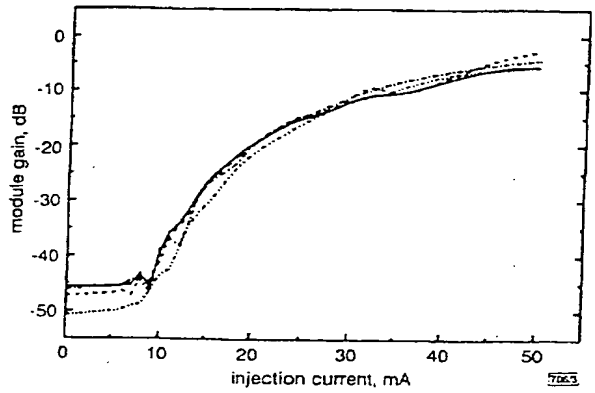


Fig. 3 *Fibre-to-fibre gain against injection current*
Input power = −10dBm

Module performances: Typical fibre-to-fibre gain against injection current is illustrated in Fig. 3. All 16 cross channels successfully perform gate operations. Insertion loss for each of these paths at an injection current of 40mA fell within the range 9 ± 4dB. Coupling loss between SOAGs and silica waveguides was estimated to be ~4.5dB. The average coupling loss between singlemode fibres and waveguides was 0.8dB, while the average 1×4 splitting loss

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was 7.4dB for each side. The intersection loss in the combiner region was <0.1 dB. Switching the injection current between 0 and 40mA resulted in an average extinction ratio of 40dB, which is large enough for optical gates to be used in a cross-talk free matrix switch [1]. Fig. 4 shows a photograph of the fabricated 4x4 optical switch module (54mm long, 22mm wide).

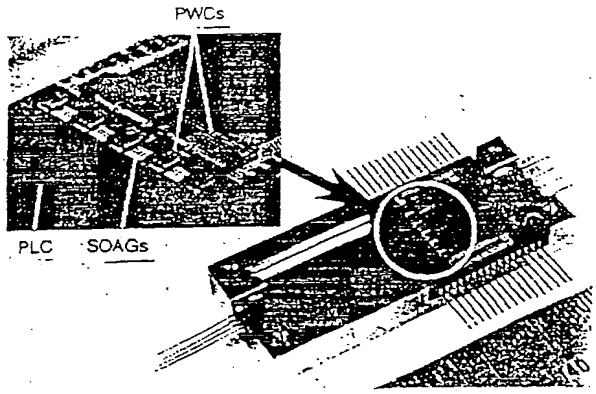

Fig. 4 *Hybrid integrated 4x4 matrix optical switch*

Summary: We have developed a hybrid integrated 4x4 matrix optical switch module, in which SSC-SOAG arrays and optical fibres are integrated on a silica based PLC platform. This integration was made possible by a newly developed self-aligned multiple chip assembly technique, using Au/Sn solder bumps and AP-CVD based PLC platform technologies.

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635nm 20mW DFB laser

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The shortest wavelength room temperature operation in an electrically pumped DFB laser is demonstrated. The InGaAlP device emits up to 20mW in a single spatial and longitudinal mode under CW conditions. Such lasers can substitute for bulky He-Ne gas lasers for meteorological and spectroscopic applications.

Introduction: DFB lasers in the InGaAlP material system present considerable advantages over their Fabry-Perot counterparts. With the lasing frequency stabilised by a buried grating, stable single longitudinal mode operation can be obtained even with changing temperature or current. The absence of the longitudinal mode hops which affect Fabry-Perot and even DBR lasers make DFBs simple to use for many applications. Reducing the wavelength to that of the red He-Ne laser allows such DFBs to replace bulky gas lasers for instrumentation and sensors. One advantage of these DFBs over He-Ne lasers is that the wavelength can be tuned over a considerable range with temperature or current. In an interferometer, this tunability allows distances to be measured without resetting the instrument, and in spectroscopic applications, the laser can be locked onto a specific narrow absorption line.

DFB lasers have previously been demonstrated in the GaInP/AlInP material system. Regrowth over a buried grating is made easier with lower aluminum concentrations, but using pure InGaP limits the wavelength to > 660nm [1–3]. Shorter wavelength operation of similar grating stabilised lasers has previously been achieved either using novel structures that do not require regrowth over the grating [4] or by cooling the device to cryogenic temperatures, or both [5].

Recently, good regrowth over aluminum containing layers in this material system has been realised, leading to 650nm DFB lasers [6]. As explained previously, this is made possible by careful cleaning of the substrate, and optimising reactor growth conditions. By further increasing the aluminum concentration, we demonstrate 630nm band operation.

Fabrication: The device structure and fabrication are similar to those of the 650nm device previously reported [6]. Strained InGaP forms the active quantum wells, where the strain is controlled to provide gain at the appropriate wavelength. The grating layer is composed of AlGaInP, whose bandgap is adjusted to be just above the lasing energy. A second order diffraction grating is formed using a holographic exposure from a 325nm HeCd laser. After wet etching, the wafer is carefully cleaned and regrown with a top *p*-type cladding. Index guided structures are formed to assure single spatial as well as single longitudinal mode operation. Cleaved bars were coated with HR on the back and AR on the front facet. The devices were then bonded *p*-down onto copper submounts and tested under CW and room temperature conditions.

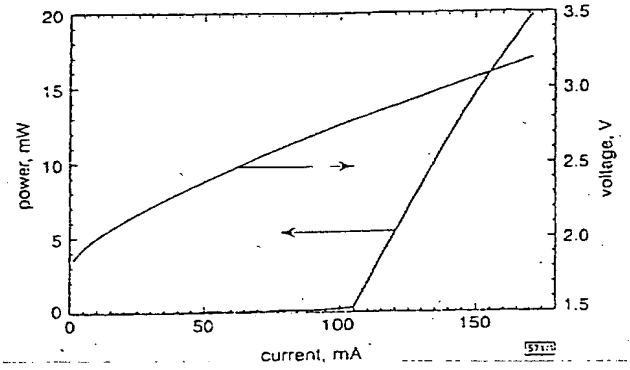

Fig. 1 *Optical power and voltage against injection current*
20°C, CW

Results: Fig. 1 shows both the operating voltage and the optical power from the device against injection current. The threshold is 105mA, with an efficiency of ~0.3W/A. The device resistance is ~5Ω, and the voltage at threshold is ~2.8V, < 1V above the